

High-Performance Processing and Visualization of High-Volume Data

HPVis

Background:

This research project is directed towards the development of a new method to improve the performance of standard PC applications by the use of algorithm implementation on FPGAs.

The project's focus lies on industrial sensor systems and image processing systems with high-volume data. The main application which is analyzed visualizes pipeline inspection measurements from the partner company Rosen TRC. During a pipeline inspection up to approximately 10^{12} measurement values are stored. They must be analyzed and visualized on a standard PC after the measurement procedure. The new method that is developed shall improve the processing performance of the underlying algorithms.

Another application field that is considered in the project is image processing. The methods investigated for the pipeline inspection application will be applied to smart cameras containing FPGAs which are produced by the partner company Visiosens.

Objectives:

1. Design of a parallel visualization framework.

A parallel data flow process model shall be developed that can be used to visualize sensor data on diverse hardware platforms with and without FPGA algorithm acceleration.

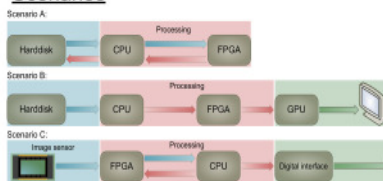
2. Implementation of the visualization framework

Implementation of the visualization framework on a standard PC platform with and without FPGA algorithm acceleration. The results of this prototype implementation shall be used to create rules for the design of PC software that runs on different hardware platforms. Reusable interfaces and hardware components will be combined to a generic optimization framework.

3. Development of innovative scaling and porting methods

The aim is to develop scaling and porting methods for combined hardware (FPGA) and software (PC) solutions. By using an optimization algorithm the porting of an application shall be done automatically according to the FPGA and PC system resource-constraints.

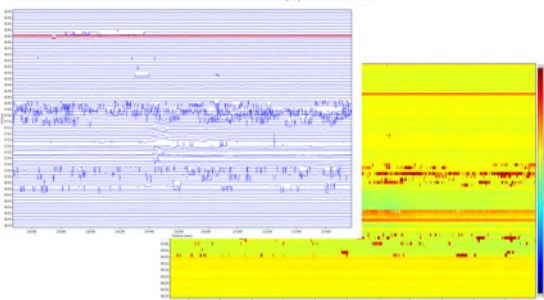
Scenarios



The following scenarios for different application classes are considered:

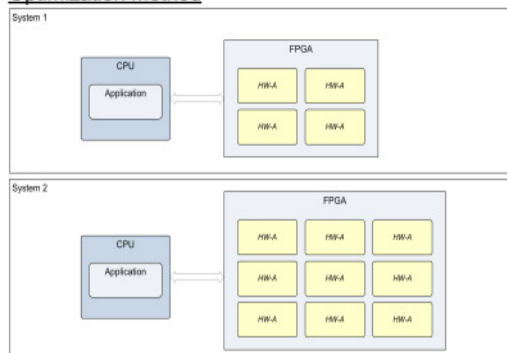
- **CPU to FPGA communication:**
Parts of the CPU Software will be implemented on the FPGA to accelerate the algorithms.
- **CPU to FPGA to GPU communication:**
Parts of the CPU Software shall be implemented on the FPGA to accelerate the algorithms. The FPGA then passes the results directly to the GPU. This scenario shall be used to effectively process and visualize high volume sensor data.
- **Image Sensor to FPGA to CPU:**
The image sensor data will be processed before it will be passed on to the CPU.

Measurement Visualization Application



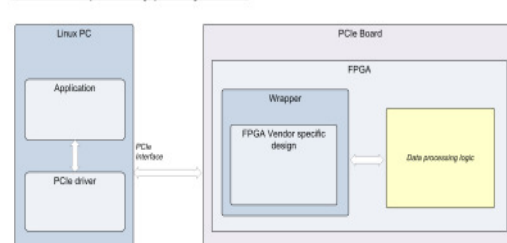
Pipeline inspection data is visualized in varying resolutions using different displaying methods.
(© Rosen RTC)

Optimization Method



The developed scaling and porting methods shall optimize the degree of parallelization depending on the hardware features of the CPU, PC main board and used PCIe FPGA card. This shall be done automatically with the knowledge of the system's boundary conditions.

Current prototype system



- PCIe driver for Linux
- PCIe Wrapper for Xilinx Spartan 6 and Xilinx Virtex 6 developed
- First test with FIR and Sobel filter as data processing logic
- Currently testing and implementing PCIe DMA capability for Linux